

CLAIM AMENDMENTS

1 1. (Currently Amended) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface and a lower surface, wherein the
3 upper surface includes a light sensitive cell and a conductive pad;
4 an insulative housing that includes a first single-piece non-transparent insulative housing
5 portion that contacts the lower surface and is spaced from the light sensitive cell and a second
6 transparent insulative housing portion that contacts the first housing portion and the light
7 sensitive cell, wherein the first housing portion includes a peripheral ledge, and the second
8 housing portion is exposed ~~located within the peripheral ledge and is exposed~~; and
9 a conductive trace that extends outside the insulative housing and is electrically
10 connected to the pad ~~inside the insulative housing~~.

1 2. (Original) The device of claim 1, wherein the first housing portion contacts four outer
2 side surfaces of the chip.

1 3. (Original) The device of claim 1, wherein the first housing portion is spaced from the
2 upper surface.

1 4. (Original) The device of claim 1, wherein the second housing portion contacts the
2 conductive trace.

1 5. (Original) The device of claim 1, wherein the second housing portion is spaced from
2 the lower surface.

1 6. (Previously Presented) The device of claim 1, wherein the second housing portion is
2 recessed relative to the peripheral ledge.

1 7. (Original) The device of claim 1, wherein the first housing portion is a transfer molded
2 material, and the second housing portion is a cured polymeric material.

1 8. (Original) The device of claim 1, wherein the conductive trace extends through a
2 peripheral side surface of the first housing portion and contacts the second housing portion
3 without extending through a surface of the second housing portion.

1 9. (Previously Presented) The device of claim 1, wherein the device is devoid of an
2 electrical conductor that extends through opposing surfaces of the second housing portion.

1 10. (Original) The device of claim 1, wherein the device is devoid of wire bonds, TAB
2 leads and solder joints.

1 11. (Currently Amended) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that contacts the lower surface and the side surfaces and is spaced from the upper surface
7 and a second transparent insulative housing portion that contacts the first housing portion and the
8 light sensitive cell and is spaced from the lower surface; and
9 a conductive trace that extends laterally through an opening in the first housing portion,
10 extends outside the insulative housing and is electrically connected to the pad inside the
11 insulative housing, wherein the first housing portion spans 360 degrees around the conductive
12 trace at the opening.

1 12. (Previously Presented) The device of claim 11, wherein the second housing portion
2 includes first and second opposing surfaces, the first surface contacts the light sensitive cell and
3 is spaced from the conductive trace, and the second surface faces away from the chip and is
4 exposed.

1 13. (Previously Presented) The device of claim 12, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within the peripheral ledge.

1 14. (Original) The device of claim 13, wherein the second housing portion is recessed
2 relative to the peripheral ledge.

1 15. (Previously Presented) The device of claim 11, wherein the first housing portion is a
2 transfer molded material, and the second housing portion is a cured polymeric material.

1 16. (Original) The device of claim 11, wherein the insulative housing consists of the first
2 and second housing portions.

1 17. (Previously Presented) The device of claim 11, wherein the first housing portion is a
2 transfer molded material that includes a peripheral ledge, and the second housing portion is a
3 cured polymeric material that is located within the peripheral ledge and includes a first surface
4 that contacts the light sensitive cell and is spaced from the conductive trace and a second surface
5 opposite the first surface that faces away from the chip and is exposed.

1 18. (Original) The device of claim 11, wherein the conductive trace extends through a
2 peripheral side surface of the first housing portion and contacts the second housing portion
3 without extending through a surface of the second housing portion.

1 19. (Previously Presented) The device of claim 11, wherein the device is devoid of an
2 electrical conductor that extends through opposing surfaces of the second housing portion.

1 20. (Original) The device of claim 11, wherein the device is devoid of wire bonds, TAB
2 leads and solder joints.

1 21. (Currently Amended) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes a top surface, a bottom surface and ~~uncurved~~
6 peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing
7 further includes first and second insulative housing portions, the first housing portion is a single-

8 piece that contacts the chip, provides the peripheral side surfaces and the bottom surface and is
9 non-transparent, and the second housing portion contacts the upper surface, is farther from the
10 bottom surface than the lower surface is from the bottom surface, does not extend across any of
11 the peripheral side surfaces, provides at least a portion of the top surface, and is transparent and
12 is exposed; and
13 a conductive trace that extends outside the insulative housing and is electrically
14 connected to the pad inside the insulative housing.

1 22. (Original) The device of claim 21, wherein the first housing portion contacts the
2 lower surface and the outer side surfaces and is spaced from the upper surface.

1 23. (Original) The device of claim 21, wherein the second housing portion contacts the
2 light sensitive cell and the conductive trace and is spaced from the lower surface.

1 24. (Original) The device of claim 21, wherein the first housing portion includes a
2 peripheral ledge that forms a peripheral portion of the top surface, and the second housing
3 portion is located within and recessed relative to the peripheral ledge.

1 25. (Previously Presented) The device of claim 21, wherein the first housing portion is a
2 transfer molded material, and the second housing portion is a cured polymeric material.

1 26. (Original) The device of claim 21, wherein the insulative housing consists of the first
2 and second housing portions.

1 27. (Previously Presented) The device of claim 21, wherein the light sensitive cell
2 contacts a major surface of the second housing portion that faces towards and is parallel to the
3 upper surface.

1 28. (Original) The device of claim 21, wherein the device is devoid of an electrical
2 conductor that extends through the top or bottom surfaces.

1 29. (Previously Presented) The device of claim 21, wherein the device is devoid of an
2 electrical conductor that extends through opposing surfaces of the second housing portion.

1 30. (Original) The device of claim 21, wherein the device is devoid of wire bonds, TAB
2 leads and solder joints.

1 31. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a top surface, a bottom surface and peripheral side
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes
7 first and second insulative housing portions, the first housing portion is a single-piece that
8 provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top
9 surface, contacts the lower surface and the outer side surfaces, is spaced from the light sensitive
10 cell and is non-transparent, and the second housing portion is a single-piece or double-piece that
11 provides a central portion of the top surface within the peripheral portion of the top surface,
12 contacts the first housing portion, the light sensitive cell and the conductive trace, is spaced from
13 the lower surface, is farther from the bottom surface than the lower surface is from the bottom
14 surface, is transparent and is exposed; and

15 a conductive trace that extends outside the insulative housing and is electrically
16 connected to the pad inside the insulative housing.

1 32. (Previously Presented) The device of claim 31, wherein the second housing portion
2 includes first and second opposing surfaces, the first surface faces towards the chip and contacts
3 the light sensitive cell and is spaced from the conductive trace, and the second surface faces away
4 from the chip and provides the central portion of the top surface and is exposed.

1 33. (Original) The device of claim 31, wherein the peripheral portion of the top surface
2 forms a rectangular peripheral ledge, and the second housing portion is located within and
3 recessed relative to the peripheral ledge.

1 34. (Original) The device of claim 33, wherein the peripheral ledge includes four inner
2 side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

1 35. (Original) The device of claim 31, wherein the first housing portion is a transfer
2 molded material, and the second housing portion is a cured polymeric material.

1 36. (Original) The device of claim 31, wherein the insulative housing consists of the first
2 and second housing portions.

1 37. (Previously Presented) The device of claim 31, wherein the first housing portion is a
2 transfer molded material that includes a peripheral ledge, and the second housing portion is a
3 cured polymeric material that is located within the peripheral ledge and includes a first surface
4 that faces towards the chip and contacts the light sensitive cell and is spaced from the conductive
5 trace and a second surface opposite the first surface that faces away from the chip and provides
6 the central portion of the top surface and is exposed.

1 38. (Original) The device of claim 31, wherein the device is devoid of an electrical
2 conductor that extends through the top or bottom surfaces.

1 39. (Previously Presented) The device of claim 31, wherein the device is devoid of an
2 electrical conductor that extends through opposing surfaces of the second housing portion.

1 40. (Original) The device of claim 31, wherein the device is devoid of wire bonds, TAB
2 leads and solder joints.

1 41. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface and a lower surface, wherein the
3 upper surface includes a light sensitive cell and a conductive pad;
4 an insulative housing that includes a top surface, a bottom surface and a peripheral side
5 surface between the top and bottom surfaces, wherein the insulative housing further includes a

6 first insulative housing portion that covers the lower surface and is non-transparent and a second
7 insulative housing portion that covers the light sensitive cell and is transparent; and
8 a conductive trace that protrudes laterally from and extends through the side surface and
9 is electrically connected to the pad, wherein the conductive trace includes a recessed portion that
10 extends into the insulative housing and is spaced from the top and bottom surfaces and a non-
11 recessed portion that extends outside the insulative housing and is adjacent to the recessed
12 portion and the top surface.

1 42. (Original) The device of claim 41, wherein the first housing portion contacts the
2 lower surface and four outer side surfaces of the chip.

1 43. (Original) The device of claim 41, wherein the second housing portion contacts the
2 light sensitive cell and the conductive trace.

1 44. (Original) The device of claim 41, wherein the first housing portion includes a
2 peripheral ledge, and the second housing portion is located within the peripheral ledge.

1 45. (Previously Presented) The device of claim 41, wherein the first housing portion is a
2 transfer molded material, and the second housing portion is a cured polymeric material.

1 46. (Original) The device of claim 41, wherein the insulative housing consists of the first
2 and second housing portions.

1 47. (Previously Presented) The device of claim 41, wherein the light sensitive cell
2 contacts a major surface of the second housing portion that faces towards and is parallel to the
3 upper surface.

1 48. (Original) The device of claim 41, wherein the device is devoid of an electrical
2 conductor that extends through the top or bottom surfaces.

1 49. (Previously Presented) The device of claim 41, wherein the device is devoid of an
2 electrical conductor that extends through opposing surfaces of the second housing portion.

1 50. (Original) The device of claim 41, wherein the device is devoid of wire bonds, TAB
2 leads and solder joints.

1 51. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface and a lower surface, wherein the
3 upper surface includes a light sensitive cell and a conductive pad;
4 an insulative housing that includes a top surface, a bottom surface and a peripheral side
5 surface between the top and bottom surfaces, wherein the insulative housing further includes a
6 first single-piece housing portion that contacts the lower surface and is spaced from the light
7 sensitive cell and a second single-piece housing portion that contacts the first housing portion
8 and the conductive trace and is transparent, the first housing portion alone provides the bottom
9 surface, and the first and second housing portions in combination provide the top surface; and
10 a conductive trace that protrudes laterally from and extends through the side surface and
11 is electrically connected to the pad, wherein the conductive trace includes a recessed portion that
12 extends into the insulative housing and is spaced from the top and bottom surfaces and a non-
13 recessed portion that extends outside the insulative housing and is adjacent to the recessed
14 portion and contacts the insulative housing, wherein the recessed and non-recessed portions each
15 include four outer surfaces, three of the outer surfaces of the recessed and non-recessed portions
16 that do not face in the same direction as the top surface are coplanar with one another where the
17 recessed and non-recessed portions are adjacent to one another, and one of the outer surfaces of
18 the recessed and non-recessed portions that face in the same direction as the top surface are not
19 coplanar with one another where the recessed and non-recessed portions are adjacent to one
20 another.

1 52. (Previously Presented) The device of claim 51, wherein the second housing portion
2 includes first and second opposing surfaces, the first surface contacts the light sensitive cell and
3 is spaced from the conductive trace, and the second surface faces away from the chip and is
4 exposed.

1 53. (Original) The device of claim 51, wherein the first housing portion includes a
2 peripheral ledge, and the second housing portion is located within and recessed relative to the
3 peripheral ledge.

1 54. (Original) The device of claim 53, wherein the peripheral ledge includes four inner
2 side surfaces that are opposite the peripheral side surfaces and outside a periphery of the chip.

1 55. (Original) The device of claim 51, wherein the first housing portion is a transfer
2 molded material, and the second housing portion is a cured polymeric material.

1 56. (Original) The device of claim 51, wherein the insulative housing consists of the first
2 and second housing portions.

1 57. (Previously Presented) The device of claim 51, wherein the first housing portion is a
2 transfer molded material that includes a peripheral ledge, and the second housing portion is a
3 polymeric material that is located within the peripheral ledge and includes a first surface that
4 contacts the light sensitive cell and is spaced from the conductive trace and a second surface
5 opposite the first surface that faces away from the chip and is exposed.

1 58. (Original) The device of claim 51, wherein the device is devoid of an electrical
2 conductor that extends through the top or bottom surfaces.

1 59. (Previously Presented) The device of claim 51, wherein the device is devoid of an
2 electrical conductor that extends through opposing surfaces of the second housing portion.

1 60. (Original) The device of claim 51, wherein the device is devoid of wire bonds, TAB
2 leads and solder joints.

1 61. (Currently Amended) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from
7 the light sensitive cell and a second transparent insulative housing portion that contacts the first
8 housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and
9 a conductive trace that extends laterally through an opening in the first housing portion,
10 extends outside the insulative housing and is electrically connected to the pad inside the
11 insulative housing, wherein the first housing portion spans 360 degrees around the conductive
12 trace at the opening.

1 62. (Previously Presented) The device of claim 61, wherein the first housing portion
2 contacts the lower surface and the side surfaces.

1 63. (Previously Presented) The device of claim 61, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within and recessed
3 relative to the peripheral ledge.

1 64. (Previously Presented) The device of claim 61, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the opening includes sidewalls that contact and span 360 degrees around the
9 recessed portion.

1 65. (Previously Presented) The device of claim 61, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 66. (Previously Presented) An optoelectronic semiconductor package device, comprising:

2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from
7 the light sensitive cell and a second transparent insulative housing portion that contacts the first
8 housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

9 a conductive trace that extends through an opening in the first housing portion, extends
10 outside the insulative housing, is bent outside the insulative housing and is electrically connected
11 to the pad inside the insulative housing.

1 67. (Previously Presented) The device of claim 66, wherein the first housing portion
2 contacts the lower surface and the side surfaces.

1 68. (Previously Presented) The device of claim 66, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within and recessed
3 relative to the peripheral ledge.

1 69. (Previously Presented) The device of claim 66, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the opening includes sidewalls that contact and span 360 degrees around the
9 recessed portion.

1 70. (Previously Presented) The device of claim 66, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 71. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from
7 the light sensitive cell and a second transparent insulative housing portion that contacts the first
8 housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and
9 a conductive trace that extends through an opening in the first housing portion, extends
10 outside the insulative housing, does not contact an insulative material outside the first housing
11 portion and is electrically connected to the pad inside the insulative housing.

1 72. (Previously Presented) The device of claim 71, wherein the first housing portion
2 contacts the lower surface and the side surfaces.

1 73. (Previously Presented) The device of claim 71, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within and recessed
3 relative to the peripheral ledge.

1 74. (Previously Presented) The device of claim 71, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the opening includes sidewalls that contact and span 360 degrees around the
9 recessed portion.

1 75. (Previously Presented) The device of claim 71, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 76. (Currently Amended) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that covers the lower surface and the side surfaces and is spaced from the light sensitive
7 cell and a second transparent insulative housing portion that contacts the first housing portion
8 and the light sensitive cell, is spaced from the lower surface and is exposed; and
9 a conductive trace that includes a lead and a planar metal trace, wherein the lead extends
10 through an opening in the first housing portion, extends outside the insulative housing, does not
11 extend across any edge of the pad and is electrically connected to the pad inside the insulative
12 housing, and the planar metal trace contacts and is not integral with the lead, contacts the first
13 housing portion, extends across one of the side surfaces and does not extend outside the
14 insulative housing.

1 77. (Previously Presented) The device of claim 76, wherein the first housing portion
2 contacts the lower surface and the side surfaces.

1 78. (Previously Presented) The device of claim 76, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within and recessed
3 relative to the peripheral ledge.

1 79. (Previously Presented) The device of claim 76, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one

8 another, and the opening includes sidewalls that contact and span 360 degrees around the
9 recessed portion.

1 80. (Previously Presented) The device of claim 76, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 81. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that covers the lower surface and the side surfaces and is spaced from the light sensitive
7 cell and a second transparent insulative housing portion that contacts the first housing portion
8 and the light sensitive cell, is spaced from the lower surface and is exposed; and

9 a conductive trace that includes a lead and a planar metal trace, wherein the lead extends
10 through an opening in the first housing portion, extends outside the insulative housing and is
11 electrically connected to the pad inside the insulative housing, and the planar metal trace contacts
12 and is not integral with the lead, contacts the first and second housing portions, extends across
13 one of the side surfaces and does not extend outside the insulative housing.

1 82. (Previously Presented) The device of claim 81, wherein the first housing portion
2 contacts the lower surface and the side surfaces.

1 83. (Previously Presented) The device of claim 81, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within and recessed
3 relative to the peripheral ledge.

1 84. (Previously Presented) The device of claim 81, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with

5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the opening includes sidewalls that contact and span 360 degrees around the
9 recessed portion.

1 85. (Previously Presented) The device of claim 81, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 86. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that covers the lower surface and the side surfaces and is spaced from the light sensitive
7 cell and a second transparent insulative housing portion that contacts the first housing portion
8 and the light sensitive cell, is spaced from the lower surface and is exposed; and
9 a conductive trace that includes a lead and a planar metal trace, wherein the lead extends
10 through an opening in the first housing portion, extends outside the insulative housing and is
11 electrically connected to the pad inside the insulative housing, and the planar metal trace contacts
12 and is not integral with the lead, contacts the first and second housing portions, overlaps the pad,
13 extends across one of the side surfaces and does not extend outside the insulative housing.

1 87. (Previously Presented) The device of claim 86, wherein the first housing portion
2 contacts the lower surface and the side surfaces.

1 88. (Previously Presented) The device of claim 86, wherein the first housing portion
2 includes a peripheral ledge, and the second housing portion is located within and recessed
3 relative to the peripheral ledge.

1 89. (Previously Presented) The device of claim 86, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the opening includes sidewalls that contact and span 360 degrees around the
9 recessed portion.

1 90. (Previously Presented) The device of claim 86, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 91. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a top surface, a bottom surface and peripheral side
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes
7 first and second insulative housing portions, the first housing portion is a single-piece that
8 contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom
9 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-
10 transparent, the second housing portion contacts the first housing portion and the light sensitive
11 cell, provides a central portion of the top surface within the peripheral portion of the top surface
12 and is transparent, and the top surface is exposed; and

13 a conductive trace that extends outside the insulative housing and is electrically
14 connected to the pad inside the insulative housing.

1 92. (Previously Presented) The device of claim 91, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 93. (Previously Presented) The device of claim 91, wherein the conductive trace extends
2 through an opening in one of the peripheral side surfaces.

1 94. (Previously Presented) The device of claim 91, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the first housing portion includes sidewalls that contact and span 360 degrees
9 around the recessed portion.

1 95. (Previously Presented) The device of claim 91, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 96. (Previously Presented) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes a top surface, a bottom surface and peripheral side
6 surfaces between the top and bottom surfaces, wherein the insulative housing further includes
7 first and second insulative housing portions, the first housing portion is a single-piece that
8 contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom
9 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-
10 transparent, the second housing portion contacts the first housing portion and the light sensitive
11 cell, provides a central portion of the top surface within the peripheral portion of the top surface
12 and is transparent, the first housing portion is exposed at the top surface, bottom surface and
13 peripheral side surfaces, and the second housing portion is exposed at the top surface; and

14 a conductive trace that extends outside the insulative housing and is electrically
15 connected to the pad inside the insulative housing.

1 97. (Previously Presented) The device of claim 96, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 98. (Previously Presented) The device of claim 96, wherein the conductive trace extends
2 through an opening in one of the peripheral side surfaces.

1 99. (Previously Presented) The device of claim 96, wherein the conductive trace includes
2 a recessed portion and a non-recessed portion, the recessed portion extends into the insulative
3 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
4 and non-recessed portions that face in the same direction as the lower surface are coplanar with
5 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
6 the recessed and non-recessed portions that face in the same direction as the upper surface are not
7 coplanar with one another where the recessed and non-recessed portions are adjacent to one
8 another, and the first housing portion includes sidewalls that contact and span 360 degrees
9 around the recessed portion.

1 100. (Previously Presented) The device of claim 96, wherein the device is devoid of wire
2 bonds, TAB leads and solder joints.

1 101. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes a top surface, a bottom surface and peripheral side
7 surfaces between the top and bottom surfaces, wherein the insulative housing further includes
8 first and second insulative housing portions, the first housing portion is a single-piece that
9 contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom
10 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-
11 transparent, the second housing portion contacts the first housing portion and the light sensitive

cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, and the top surface is exposed; and
a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

102. (Previously Presented) The device of claim 101, wherein the first housing portion contacts the lower surface and the outer side surfaces.

103. (Previously Presented) The device of claim 101, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

104. (Previously Presented) The device of claim 101, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

105. (Previously Presented) The device of claim 101, wherein the device is devoid of wire bonds, TAB leads and solder joints.

106. (Previously Presented) An optoelectronic semiconductor package device, comprising:
a semiconductor chip that includes an upper surface, a lower surface and four outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a top surface, a bottom surface and peripheral side surfaces between the top and bottom surfaces, wherein the insulative housing further includes first and second insulative housing portions, the first housing portion is a single-piece that contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-transparent, the second housing portion contacts the first housing portion and the light sensitive cell, provides a central portion of the top surface within the peripheral portion of the top surface and is transparent, the central portion of the top surface is recessed relative to the peripheral portion of the top surface, the first housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed at the top surface; and a conductive trace that extends outside the insulative housing and is electrically connected to the pad inside the insulative housing.

107. (Previously Presented) The device of claim 106, wherein the first housing portion contacts the lower surface and the outer side surfaces.

108. (Previously Presented) The device of claim 106, wherein the conductive trace extends through an opening in one of the peripheral side surfaces.

109. (Previously Presented) The device of claim 106, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the first housing portion includes sidewalls that contact and span 360 degrees around the recessed portion.

110. (Previously Presented) The device of claim 106, wherein the device is devoid of wire bonds, TAB leads and solder joints.

1 111. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:
3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;
6 an insulative housing that includes a top surface, a bottom surface and peripheral side
7 surfaces between the top and bottom surfaces, wherein the insulative housing further includes
8 first and second insulative housing portions, the first housing portion is a single-piece that
9 contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom
10 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-
11 transparent, the second housing portion contacts the first housing portion and the light sensitive
12 cell, provides a central portion of the top surface within the peripheral portion of the top surface
13 and is transparent, and the top, bottom and peripheral side surfaces are exposed; and
14 a conductive trace that extends outside the insulative housing, is located between the
15 second housing portion and the chip inside the insulative housing, is spaced from the top surface
16 and is electrically connected to the pad inside the insulative housing.

1 112. (Previously Presented) The device of claim 111, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 113. (Previously Presented) The device of claim 111, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 114. (Previously Presented) The device of claim 111, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are

8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 115. (Previously Presented) The device of claim 111, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 116. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes a top surface, a bottom surface and peripheral side
7 surfaces between the top and bottom surfaces, wherein the insulative housing further includes
8 first and second insulative housing portions, the first housing portion is a single-piece that
9 contacts the chip, covers the lower surface and the outer side surfaces and provides the bottom
10 surface, the peripheral side surfaces and a peripheral portion of the top surface and is non-
11 transparent, the second housing portion contacts the first housing portion and the light sensitive
12 cell, provides a central portion of the top surface within the peripheral portion of the top surface
13 and is transparent, and the top, bottom and peripheral side surfaces are exposed; and

14 a conductive trace that extends outside the insulative housing, includes a top surface that
15 faces away from the chip and contacts the second housing portion inside the insulative housing,
16 includes a bottom surface that faces towards the chip and contacts the second housing portion
17 inside the insulative housing, is spaced from the top and bottom surfaces, extends through one of
18 the peripheral side surfaces and is electrically connected to the pad inside the insulative housing.

1 117. (Previously Presented) The device of claim 116, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 118. (Previously Presented) The device of claim 116, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 119. (Previously Presented) The device of claim 116, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 120. (Previously Presented) The device of claim 116, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 121. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes first and second insulative housing portions, wherein
7 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces
8 and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom
9 surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge
10 opposite the peripheral side surfaces that extend from the top surface towards the bottom surface
11 and are spaced from the bottom surface and is non-transparent, and the second housing portion is
12 located within and recessed relative to the peripheral ledge, contacts the light sensitive cell, does
13 not extend midway between the upper and lower surfaces outside the chip and is transparent; and

14 a conductive trace that extends outside the insulative housing and is electrically
15 connected to the pad inside the insulative housing.

1 122. (Previously Presented) The device of claim 121, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 123. (Previously Presented) The device of claim 121, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 124. (Previously Presented) The device of claim 121, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 125. (Previously Presented) The device of claim 121, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 126. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes first and second insulative housing portions, wherein
7 the first housing portion is a single-piece that includes a top surface, a bottom surface, peripheral
8 side surfaces between the top and bottom surfaces, a peripheral ledge at the top surface, and inner
9 side surfaces inside the peripheral ledge opposite the peripheral side surfaces that extend from
10 the top surface towards the bottom surface and are spaced from the bottom surface and is non-
11 transparent, the second housing portion is located within and recessed relative to the peripheral
12 ledge, contacts the light sensitive cell, does not extend midway between the upper and lower
13 surfaces outside the chip and is transparent, the first housing portion is exposed at the top

14 surface, bottom surface and peripheral side surfaces, and the second housing portion is exposed
15 at the top surface; and

16 a conductive trace that extends outside the insulative housing and is electrically
17 connected to the pad inside the insulative housing.

1 127. (Previously Presented) The device of claim 126, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 128. (Previously Presented) The device of claim 126, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 129. (Previously Presented) The device of claim 126, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 130. (Previously Presented) The device of claim 126, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 131. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes first and second insulative housing portions, wherein
7 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces

8 and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom
9 surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge
10 opposite the peripheral side surfaces that extend from the top surface towards the bottom surface
11 and are spaced from the bottom surface and is non-transparent, and the second housing portion is
12 located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and
13 the inner side surfaces, does not extend midway between the upper and lower surfaces outside the
14 chip and is transparent; and

15 a conductive trace that extends outside the insulative housing and is electrically
16 connected to the pad inside the insulative housing.

1 132. (Previously Presented) The device of claim 131, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 133. (Previously Presented) The device of claim 131, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 134. (Previously Presented) The device of claim 131, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 135. (Previously Presented) The device of claim 131, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 136. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes first and second insulative housing portions, wherein
7 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces
8 and includes a top surface, a bottom surface, peripheral side surfaces between the top and bottom
9 surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the peripheral ledge
10 opposite the peripheral side surfaces that extend from the top surface towards the bottom surface
11 and are spaced from the bottom surface and is non-transparent, the second housing portion is
12 located within and recessed relative to the peripheral ledge, contacts the light sensitive cell and
13 the inner side surfaces, does not extend midway between the upper and lower surfaces outside the
14 chip and is transparent, the first housing portion is exposed at the top surface, bottom surface and
15 peripheral side surfaces, and the second housing portion is exposed at the top surface; and

16 a conductive trace that extends outside the insulative housing and is electrically
17 connected to the pad inside the insulative housing.

1 137. (Previously Presented) The device of claim 136, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 138. (Previously Presented) The device of claim 136, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 139. (Previously Presented) The device of claim 136, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 140. (Previously Presented) The device of claim 136, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 141. (Currently Amended) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

5 an insulative housing that includes first and second insulative housing portions, wherein
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces
7 and includes a top surface, a bottom surface, ~~uneurved~~ peripheral side surfaces between the top
8 and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the
9 peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards
10 the bottom surface and are spaced from the bottom surface and is non-transparent, and the second
11 housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not
12 extend midway between the upper and lower surfaces outside the chip, does not extend across
13 any of the peripheral side surfaces, and is transparent and is exposed; and

14 a conductive trace that extends outside the insulative housing and is electrically
15 connected to the pad inside the insulative housing.

1 142. (Previously Presented) The device of claim 141, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 143. (Previously Presented) The device of claim 141, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 144. (Previously Presented) The device of claim 141, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one

6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 145. (Previously Presented) The device of claim 141, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 146. (Previously Presented) An optoelectronic semiconductor package device,
2 comprising:

3 a semiconductor chip that includes an upper surface, a lower surface and four outer side
4 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
5 sensitive cell and a conductive pad;

6 an insulative housing that includes first and second insulative housing portions, wherein
7 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces
8 and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top
9 and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the
10 peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards
11 the bottom surface and are spaced from the bottom surface and is non-transparent, the second
12 housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not
13 extend midway between the upper and lower surfaces outside the chip and is transparent, the first
14 housing portion is exposed at the top surface, bottom surface and peripheral side surfaces, and
15 the second housing portion is exposed at the top surface; and

16 a conductive trace that extends outside the insulative housing and is electrically
17 connected to the pad inside the insulative housing.

1 147. (Previously Presented) The device of claim 146, wherein the first housing portion
2 contacts the lower surface and the outer side surfaces.

1 148. (Previously Presented) The device of claim 146, wherein the conductive trace
2 extends through an opening in one of the peripheral side surfaces.

1 149. (Previously Presented) The device of claim 146, wherein the conductive trace
2 includes a recessed portion and a non-recessed portion, the recessed portion extends into the
3 insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of
4 the recessed and non-recessed portions that face in the same direction as the lower surface are
5 coplanar with one another where the recessed and non-recessed portions are adjacent to one
6 another, surfaces of the recessed and non-recessed portions that face in the same direction as the
7 upper surface are not coplanar with one another where the recessed and non-recessed portions are
8 adjacent to one another, and the first housing portion includes sidewalls that contact and span
9 360 degrees around the recessed portion.

1 150. (Previously Presented) The device of claim 146, wherein the device is devoid of
2 wire bonds, TAB leads and solder joints.

1 151. (New) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes a first single-piece non-transparent insulative housing
6 portion that contacts the lower surface and the side surfaces and is spaced from the upper surface
7 and a second transparent insulative housing portion that contacts the first housing portion and the
8 light sensitive cell, is spaced from the lower surface and is recessed relative to the peripheral
9 ledge; and
10 a conductive trace that extends through an opening in the first housing portion, extends
11 outside the insulative housing and is electrically connected to the pad inside the insulative
12 housing.

1 152. (New) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that contacts the chip, covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and a conductive trace that extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, wherein the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that face in the same direction as the lower surface are coplanar with one another where the recessed and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed portions that face in the same direction as the upper surface are not coplanar with one another where the recessed and non-recessed portions are adjacent to one another, and the opening includes sidewalls that contact and span 360 degrees around the recessed portion.

153. (New) An optoelectronic semiconductor package device, comprising:

a semiconductor chip that includes an upper surface, a lower surface and outer side surfaces between the upper and lower surfaces, wherein the upper surface includes a light sensitive cell and a conductive pad;

an insulative housing that includes a first single-piece non-transparent insulative housing portion that covers the lower surface and the side surfaces and is spaced from the light sensitive cell and a second transparent insulative housing portion that contacts the first housing portion and the light sensitive cell, is spaced from the lower surface and is exposed; and

a conductive trace that includes a lead and a planar metal trace, wherein the lead extends through an opening in the first housing portion, extends outside the insulative housing and is electrically connected to the pad inside the insulative housing, the planar metal trace contacts and is not integral with the lead, extends across one of the side surfaces and does not extend outside the insulative housing, and the conductive trace includes a recessed portion and a non-recessed portion, the recessed portion extends into the insulative housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed and non-recessed portions that

16 face in the same direction as the lower surface are coplanar with one another where the recessed
17 and non-recessed portions are adjacent to one another, surfaces of the recessed and non-recessed
18 portions that face in the same direction as the upper surface are not coplanar with one another
19 where the recessed and non-recessed portions are adjacent to one another, and the opening
20 includes sidewalls that contact and span 360 degrees around the recessed portion.

1 154. (New) An optoelectronic semiconductor package device, comprising:
2 a semiconductor chip that includes an upper surface, a lower surface and four outer side
3 surfaces between the upper and lower surfaces, wherein the upper surface includes a light
4 sensitive cell and a conductive pad;
5 an insulative housing that includes first and second insulative housing portions, wherein
6 the first housing portion is a single-piece that covers the lower surface and the outer side surfaces
7 and includes a top surface, a bottom surface, uncurved peripheral side surfaces between the top
8 and bottom surfaces, a peripheral ledge at the top surface, and inner side surfaces inside the
9 peripheral ledge opposite the peripheral side surfaces that extend from the top surface towards
10 the bottom surface and are spaced from the bottom surface and is non-transparent, and the second
11 housing portion extends into the peripheral ledge, contacts the light sensitive cell, does not
12 extend midway between the upper and lower surfaces outside the chip and is transparent; and
13 a conductive trace that extends outside the insulative housing and is electrically
14 connected to the pad inside the insulative housing, wherein the conductive trace includes a
15 recessed portion and a non-recessed portion, the recessed portion extends into the insulative
16 housing, the non-recessed portion extends outside the insulative housing, surfaces of the recessed
17 and non-recessed portions that face in the same direction as the lower surface are coplanar with
18 one another where the recessed and non-recessed portions are adjacent to one another, surfaces of
19 the recessed and non-recessed portions that face in the same direction as the upper surface are not
20 coplanar with one another where the recessed and non-recessed portions are adjacent to one
21 another, and the first housing portion includes sidewalls that contact and span 360 degrees
22 around the recessed portion.